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09/524,408	03/13/2000	Kanad Chakraborty	YO999-598	7403

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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	15

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/524,408	Applicant(s) CHAKRABORTY ET AL.	
	Examiner Eduardo Garcia-Otero	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: First Action after RCE

Introduction

1. Title is: METHOD AND APPARATUS FOR APPLYING FINE GRAINED TRANSFORMS DURING PLACEMENT SYNTHESIS INTERACTION
2. First named inventor is: CHAKRABORTY
3. Claims 1-39 have been submitted, examined, and rejected.
4. The independent claims are: 1, 16, 21, 22, 37-39.
5. This action is in reply to Applicant's Amendment filed 4/9/04, and Request for Continued Examination (RCE) filed 4/29/04. Claims 1-13, 15-34, and 36-39 have been amended.
6. US Application was filed 03/13/00, and there are no claims for earlier priority.

Index of Prior Art

7. **Shenoy** refers to US Patent 6,378,114.

Discussion of Specification and Drawings

8. A preliminary discussion of the specification and drawings is useful as a background for the rejections.
9. THREE SEPARATE DOMAINS. Applicant presents an interesting broad conceptual approach to integrated circuit design, whereby the circuit design space (the universe of all possible circuit designs) is defined by three separate domains at Specification page 5 lines 3-4: "in Figure 1, the three axes represent optimizations along Boolean, electrical and physical domains". Said broad conceptual approach is very useful for broad conceptual or theoretical discussions.
10. However, Applicant's broad representation of circuit design space has limited direct application in a practical optimization environment, because the three domains interact in a complex, non-linear, and unpredictable fashion. See Shenoy Column 1. Optimizing in one domain generally degrades another domain in a non-linear and unpredictable complex fashion. For example, circuit elements (transistors) with larger areas are faster (electrical domain), but take more layout area (physical domain). Thus, Applicant's representation of the prior art's sequential optimization as traveling sequentially from point to point in directions parallel with the axes (specification page 5 and FIG 1 points A-F) is not fully accurate because the axes are interactive.

11. Note that optimization in a single domain will simultaneously affect the other domains. For example, the electrical and physical domains are directly related, as discussed in the transistor example above. The Boolean domain is slightly different because the electrical and physical domains may be changed without changing the Boolean domain. However, any change in the Boolean domain will always change both the physical and electrical domains. See Shenoy column 1.
12. Further, Specification page 9 line 17 states that "a single step may optimize the physical, Boolean and electrical dimensions, thus moving the design from point A to F' in the design space. Multiple steps are not required". This broad assertion is not supported. Consider a simple illustrative example: first the Boolean space is changed, then this change is propagated to the electrical domain (new electrical elements to implement the new Boolean logic, and new basic characteristics of the new electrical elements), and then propagated to the physical (layout) domain, and then propagated to the electrical domain again (capacitance of connecting lines, noise from connecting lines, and related electrical characteristics that are dependent upon the layout of the electrical elements). See Shenoy column 1. This simple example illustrates the key point that changes to a single domain must be propagated sequentially to the other domains, and that the "overall design" (Shenoy column 1 line 66) is optimized, and all three domains are not optimized simultaneously.
13. COMPLEXITY OF INTEGRATED CIRUITS. Modern integrated circuits are probably the most complex creations of man. They contain millions of individual electrical elements, tightly packed into three dimensions, with electric charges generating electric fields, and with moving charges generating magnetic fields, with heat being generated and dissipated, with logical operations occurring, and with all of these chemical, electrical, logical, quantum semiconductor, and thermal phenomenon interacting in space and in time at frequencies of millions or billions of cycles per second. Thus, the design and optimization of integrated circuits is highly unpredictable. See the Wands 8 factor test regarding undue experimentation, particularly factor (7) "the predictability or unpredictability of the art", *In re Wands* (CA FC) 8 USPQ2d 1400, 1404 (9/30/1998).

Applicant's Remarks

14. 35 USC 101 REJECTIONS. The prior 35 USC 101 rejections are withdrawn due to Applicant's amendments.
15. 35 USC 112 FIRST AND SECOND PARAGRAPH REJECTIONS. The prior 35 USC 112 rejections are withdrawn due to Applicant's amendments.
16. 35 USC 102 REJECTIONS. Applicant Remarks page 12-14 discuss Shenoy. Applicant asserts that Shenoy only discloses a single step, whereas the instant claims require "a plurality of steps which are applied in a flexible sequence". Emphasis in original. The term "flexible" occurs in the Abstract of the instant Application ("flexible mechanism"). The concept of flexible optimization appears implicit in complex multiple criteria optimization problem. The integrated circuit design process may accurately be described as a multiple criteria (factor) optimization problem, see Shenoy column 1 line 66 "overall design...". Unfortunately, typically it is impossible to simultaneously optimize each of the individual multiple criteria. For example, larger gates (or additional buffers) will speed the signal processing (good), but larger gates will also take more space and consume more power (bad). Further, the complex interactions between size and speed and power require complex iterative search procedures during optimization. See Shenoy FIG 1 for an iterative multiple step search procedure for an optimal design.
17. To summarize, the instant claim term "flexible" is interpreted as "iterative", and is disclosed by Shenoy's iterations, see Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design". See Shenoy FIG 1.
18. Applicant further emphasizes the term "sequences", stating "sequences that do not improve the design space are rejected". Said "sequences" appear disclosed by Shenoy's iterations.
19. The prior art rejections have been amended slightly to match the claim amendments. See below.

35 USC § 102(e): filed before 11/29/00 and not vol. pub. under 35 USD 122(b)

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a

patent unless – (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

21. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).
22. **Claims 1-39 are rejected under 35 U.S.C. 102(e)** as anticipated by Shenoy US Patent 6,378,114.
23. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by Shenoy US Patent 6,378,114.
24. Claim 1 is an independent "method" claim with 4 limitations, labeled by the Examiner for clarity.
25. [1] **"selectively applying a set of steps of placement and netlist modification transforms in a flexible sequence, each transform including a plurality of steps"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
26. [2] **"evaluating the impact of the sequence of the set of steps of the modification transforms on the design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design" , and FIG 1.
27. [3] **"rejecting evaluated sequences that do not improve the design space"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse

in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design" , and FIG 1.

28. [4] **"repeating the above to create a design process flow to meet design performance targets"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
29. Claims 2-15 depend from claim 1, and are rejected below.
30. In claim 2, **"selectively applying starts from a netlist without an initial placement of said circuit or from a netlist with an initial placement"** is disclosed by Shenoy at column 1 line 31 "the synthesis program generates a netlist... Next, a physical design tool is used".
31. In claim 3, "**said placement and netlist modification transforms are divided into a set of steps each addressing a specific phase of the placement and synthesis process"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1, and column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions". Applicant Remarks received 10/23/03 define the term "decomposed" as "division of a larger item into a series of smaller items".
32. In claim 4, **"steps of the placement transforms are selectively mixed and matched with steps of logic synthesis transforms"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
33. In claim 5, **"a single sequence of sets of steps of the transforms optimizes the combination of the physical, Boolean and electrical domain, thus moving the design from a start point to an end point in the design space"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large,

complicated circuits into a multitude of simpler functions", and column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design".

34. In claim 6, **"a single sequence of sets of steps of the transforms affects multiple objectives and constraints which involve physical placement, electrical properties, and logical data"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design" , and FIG 1.
35. In claim 7, **"a partially placed and synthesized design is a starting point of said method"** is disclosed by Shenoy at column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
36. In claim 8, **"said process flow comprises a single flow of successive application of a set of steps of the transforms until design performance targets are met"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
37. In claim 9, **"utilizing an infrastructure of bins, and wherein a congestion analysis is based on the bins"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
38. In claim 10, **"placement and netlist changes are performed in said transforms"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might

sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

39. In claim 11, **"transforms are organized together in flexible scenarios to achieve a design closure process"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
40. In claim 12, **"at predetermined stages of the process, selectively determining whether to intercept the process and implement any of a plurality of transforms"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
41. In claim 13, **"examining a plurality of domains to find an improved design, said examining comprising creating a sequence of steps of placement and netlist modification transforms, to create a design closure process meeting design performance targets"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
42. In claim 14, **"all transforms have a unified view of the placement and synthesis design space"** is disclosed by Shenoy column 1 lines 18-20 which states "computers can be programmed to reduce or decompose large, complicated circuits into a multitude of simpler functions". Applicant Remarks received 12/23/03 define "unified view" as "common database repository and application programming interface for all data regarding the design -- Boolean, electrical, and physical". One of ordinary skill in the art would interpret Shenoy's "computers" as disclosing a common database for all data regarding the design, because using a common database simplifies performing the requisite iterative design steps.
43. In claim 15, **"synthesis timing, and placement data are all concurrently available to said transforms, such that said transforms modify a netlist and placement"** is disclosed by

Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

44. Claim 16 is an independent "method" claim with 6 limitations, labeled (a)-(f) by Applicant:
45. (a)-**"creating and updating bins"**
46. (b)-**"applying a plurality of transforms on a bin-based database updated by both placement and synthesis, each transform including a plurality of steps"**
47. (c)-**"updating the bin-based timing, and invoking a synthesis-placement scenario"**
48. (d)-**"selecting synthesis and placement transforms"**
49. (e)-**"invoking steps of selected transforms within said scenario using a driver"**
50. (f)-**"applying transforms that change the physical, electrical, and Boolean logic design space"**
51. Limitations (a)-(f) are disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1. Note that Shenoy FIG 1 uses the term "partitions".
52. Claims 17-20 depend from claim 16.
53. In claim 17, **"repeating (a) through (f) until design performance targets are met"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
54. In claim 18, **"a design space is moved from one point to another by considering subsets of Boolean transforms, electrical transforms, and physical transforms"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

55. In claim 19, **"steps of the transforms are interspersed sequentially"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
56. In claim 20, **"each of said transforms is represented as plurality of transformations such tat the transforms are divided into steps and the steps are iterspsed sequentially, to examine and improve each of the Boolean, electrical and physical domains"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.
57. Claim 21 is an independent "method" claim with 8 limitations, labeled [1] to [8] by Examiner.
58. [1]-**"creating and updating bins"**
59. [2]-**"applying the transforms on a bin-based database updated by both placement and synthesis"**
60. [3]-**"updating the bin-based timing"**
61. [4]-**"invoking a synthesis-placement script based on said placement and said synthesis"**
62. [5]-**"selecting synthesis and placement transforms"**
63. [6]-**"invoking selected transforms within said synthesis-placement script"**
64. [7]-**"applying transforms that change the physical, electrical, and Boolean logic design space"**
65. [8]-**"repeating the above until design performance targets are met"**
66. Limitations [1] to [8] are disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1. Note that Shenoy FIG 1 uses the term "partitions".

67. Claim 22 is an independent "system" claim with 3 limitations, labeled by the Examiner for clarity.

68. [1] **"a unit for selectively applying a sequence of steps of placement and netlist modification transforms, each transform including a plurality of steps"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

69. [2] **"a unit to evaluate the impact of the sequence of steps of the modifications transforms on the design space and to reject evaluated sequences that do not improve the design space to create a design process flow meeting performance targets"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

70. [3] **"said transforms allow selective mixing and matching of the steps of the transforms to optimize the placement of a circuit in a design space"** is disclosed by Shenoy column 1 line 54 "several iterations... to optimize... each of these stages is highly dependent on the results of the other stages... the overall design might sometimes be worse in a successive iteration", and column 3 line 32 "after cell separation is performed, the netlist is tweaked to optimize the design", and FIG 1.

71. Claims 23-36 depend from claim 22, with the same additional limitations as "method" claims 2-15, and are rejected for the same reasons.

72. Claim 37 is an independent "software system" claim, with the same limitations as "system" claim 22, and is rejected for the same reasons.

73. Claims 38 and 39 are "programmable storage medium" claims with the same limitations as "method" claims 1-15 above, and are rejected for the same reason.

Conclusions

74. All claims 1-39 stand rejected.

Communication

75. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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